What is claimed is:

1. A circuit for down-converting a differential input signal x(t) comprising:

a differential transconductance input cell consisting of separate positive and negative channels for receiving positive and negative channels of said input signal x(t) and amplifying said positive and negative channels of said input signal x(t);

a first differential mixer for receiving said amplified input signal x(t), and mixing said input signal x(t) with a first mixing signal φ1, to generate an output signal φ1 x(t);

a second differential mixer for receiving said signal φ1 x(t) as an input, and mixing said signal φ1 x(t) with a second mixing signal φ2, to generate an output signal φ1 φ2 x(t);

a pair of current sources Ia and Ib for providing current to respective outputs of said positive and negative channels of said differential transconductance input cell, to reduce the current drawn from said first differential mixer, said current sources Ia and Ib being trimmed in a complementary manner where $Ia = I + \Delta I$, and $Ib = I - \Delta I$.

2. The circuit of claim 1 further comprising means for setting the level of ΔI.

3. The circuit of claim 1 further comprising means for manipulating ΔI to reduce the IM2 and DC offset in the output signal φ1 φ2 x(t), whereby matching parameters for said mixers can be relaxed.

4. The circuit of claim 1 wherein ΔI is determined during a two-tone test, as the current level which minimizes IM2 output at baseband.

5. The circuit of claim 1 wherein said first mixing signal φ1 and said second mixing signal φ2 are chosen to demodulate said input signal x(t) to baseband.

6. The circuit of claim 3 further comprising a filter electrically connected between said first mixer and said second mixer.

7. The circuit of claim 4 wherein said filter comprises a high pass filter.

8. The circuit of claim 1, where said first mixing signal φ1 and said second mixing signal φ2 are chosen to emulate a direct conversion local oscillator signal, where φ1 * φ2 has significant power at the frequency of said local oscillator signal being emulated, and neither of said φ1 nor said φ2 having significant power at the carrier frequency of said input signal x(t) or said LO signal being emulated.

9. The circuit of claim 6, where said first mixing signal φ1 is a multi-tonal signal, and said second mixing signal φ2 is a monotonal signal.

10. The circuit of claim 1 wherein:

each of said current sources Ia and Ib comprises a plurality of switchable transistors, each with different performance parameters; and

said circuit further comprises a means for switching the various transistors in and out of the circuit to vary the current supplied.

11. The circuit of claim 1 wherein the output of each of said current sources Ia and Ib is modulated using a common mode feedback circuit.

12. The circuit of claim 10 wherein said first mixer comprises an active mixer.

13. The circuit of claim 14 wherein said first mixer comprises an active mixer having adjustable performance.

14. The circuit of claim 20 wherein said second mixer comprises a passive mixer.

15. The circuit of claim 22, wherein said high pass filter comprises a resistor dividing network for setting the common mode voltage output.

16. The circuit of claim 5 wherein said first mixing signal and said second mixing signal are generated by a voltage-controlled oscillator.

17. The circuit of claim 6 wherein said voltage-controlled oscillator is tuned to a multiple of the carrier frequency of said input signal x(t).

18. The circuit of claim 6 wherein said voltage-controlled oscillator is tuned to a divisor of the carrier frequency of said input signal x(t).

19. A method of signal demodulation for a circuit having

a differential transconductance input cell consisting of separate positive and negative channels for receiving positive and negative channels of said input signal x(t) and amplifying said positive and negative channels of said input signal x(t);

a first differential mixer for receiving said amplified input signal x(t), and mixing said input signal x(t) with a first mixing signal φ1, to generate an output signal φ1 x(t);

a second differential mixer for receiving said signal φ1 x(t) as an input, and mixing said signal φ1 x(t) with a second mixing signal φ2, to generate an output signal φ1 φ2 x(t);

a pair of current sources Ia and Ib for providing current to respective ones of said positive and negative channels of said differential transconductance input cell, to reduce the drawn from said first differential mixer;

said current sources Ia and Ib being trimmed in a complementary manner where Ia = I + ΔI, and Ib = I - ΔI;

said method comprising the steps of:

injecting a two-tone signal at said input;

measuring IM2 at the baseband output of said circuit;

determining the level of ΔI which minimizes IM2;

recording the level of ΔI which minimizes IM2; and

using said recorded level of ΔI during normal operation of said down-convertor.

20. A method of down-converting a differential input signal x(t) comprising the steps of:

amplifying positive and negative channels of said input signal x(t) using a differential transconductance input cell consisting of separate positive and negative channels;

mixing said amplified input signal x(t) with a first mixing signal φ1, to generate an output signal φ1 x(t), using a first differential mixer;.

mixing said signal φ1 x(t) with a second mixing signal φ2, to generate an output

signal φ1 φ2 x(t), using a second differential mixer; and

providing current to respective ones of said positive and negative channels of said differential transconductance input cell, using a pair of current sources Ia and Ib, reducing the current drawn from said first differential mixer; and

trimming said current sources Ia and Ib in a complementary manner where $Ia = I + \Delta I$, and $Ib = I - \Delta I$;

wherein ΔI can be manipulated to reduce the IM2 and DC offset in the output signal φ1 φ2 x(t), and wherein matching parameters for said mixers can be relaxed.

21. A computer readable memory medium for storing software code executable to perform the method steps of claim 29.

22. A computer readable memory medium for storing hardware development code to fabricate the device of any one of claims 1 through 28.